WHAT IS CLAIMED IS:

1. An apparatus having a transfer mode abnormality detecting function comprising:

at least two modules connected to each other through an interface bus in at least two different modes so that data can be transferred between said modules;

a determining means for determining whether or not a basic mode predetermined between said at least two different modes agrees with a mode set in a mode setting sequence executed when said apparatus is reset or when data is transferred between said modules; and

a notifying means for determining that transfer mode abnormality occurs when said determining means determines that said modes do not agree with each other, and for notifying of an error notice.

2. The apparatus having a transfer mode abnormality detecting function according to claim 1 further comprising:

a controlling means for rerunning said mode setting sequence in response to said error notice from said notifying means.

3. The apparatus having a transfer mode abnormality

detecting function according to claim 2, wherein when said determining means again determines that said modes do not agree with each other after said controlling means reruns said mode setting sequence, said notifying means determines that a failure occurs and notifies of a failure notice.

4. The apparatus having a transfer mode abnormality detecting function according to claim 1, wherein said determining means determines that said modes do not agree with each other when a confirmation signal responding to said basic mode remains disabled at the time of executing said mode setting sequence.

5. The apparatus having a transfer mode abnormality detecting function according to claim 1, wherein said interface bus is a PCI (Peripheral Component Interconnect) bus.

6. The apparatus having a transfer mode abnormality detecting function according to claim 2, wherein said interface bus is a PCI (Peripheral Component Interconnect) bus.

7. The apparatus having a transfer mode abnormality detecting function according to claim 3, wherein said interface bus is a PCI (Peripheral Component

Interconnect) bus.

8. The apparatus having a transfer mode abnormality detecting function according to claim 4, wherein said interface bus is a PCI (Peripheral Component Interconnect) bus.

9. The apparatus having a transfer mode abnormality detecting function according to claim 5, wherein said interface bus is a 64-bit PCI bus, said at least two different modes are a 64-bit transfer mode and a 32-bit transfer mode, said basic mode is said 64-bit transfer mode; and

when said determining means determines that said modes do not agree with each other, said notifying means determines that an inefficient transfer status occurs as said transfer mode abnormality, and notifies of said error notice.

10. The apparatus having a transfer mode abnormality detecting function according to claim 6, wherein said interface bus is a 64-bit PCI bus, said at least two different modes are a 64-bit transfer mode and a 32-bit transfer mode, said basic mode is said 64-bit transfer mode; and

when said determining means determines that said modes do not agree with each other, said notifying

means determines that an inefficient transfer status occurs as said transfer mode abnormality, and notifies of said error notice.

11. The apparatus having a transfer mode abnormality detecting function according to claim 7, wherein said interface bus is a 64-bit PCI bus, said at least two different modes are a 64-bit transfer mode and a 32-bit transfer mode, said basic mode is said 64-bit transfer mode; and

when said determining means determines that said modes do not agree with each other, said notifying means determines that an inefficient transfer status occurs as said transfer mode abnormality, and notifies of said error notice.

12. The apparatus having a transfer mode abnormality detecting function according to claim 8, wherein said interface bus is a 64-bit PCI bus, said at least two different modes are a 64-bit transfer mode and a 32-bit transfer mode, said basic mode is said 64-bit transfer mode; and

when said determining means determines that said modes do not agree with each other, said notifying means determines that an inefficient transfer status occurs as said transfer mode abnormality, and notifies of said error notice.

13. A storage controlling apparatus disposed between a disk unit and a host to control an access from said host to said unit, said storage controlling apparatus comprising:

a disk interface module for controlling an interface with said disk unit;

a host interface module for controlling an interface with said host;

a management module for generally managing the whole of said apparatus;

a bridge module connected said disk interface module, said host interface module and said management module through interface buses to connect said disk interface module, said host interface module and said management module to one another so that data can be transferred among said disk interface module, said host interface module and said management module;

said disk interface module, said host interface module, said management module and said bridge module being connected in at least two different modes so that data can be transferred among said disk interface module, said host interface module, said management module and said bridge module;

a determining means for determining whether or not a basic mode predetermined between said at least two different modes agrees with a mode set in a mode

setting sequence executed when said storage controlling apparatus is reset or when data is transferred among said modules; and

a notifying means for determining that transfer mode abnormality occurs when said determining means determines that said modes do not agree with each other, and for notifying of an error notice.

14. The storage controlling apparatus according to claim 13 further comprising:

a controlling means for rerunning said mode setting sequence when receiving said error notice from said notifying means.

15. The storage controlling apparatus according to claim 14, wherein when said determining means again determines that said modes do not agree with each other after said controlling means reruns said mode setting sequence, said notifying means determines that a failure occurs and notifies of a failure notice.

16. The storage controlling apparatus according to claim 13, wherein said determining means determines that said modes do not agree with each other when a confirmation signal responding to said basic mode remains disabled at the time of executing said mode

setting sequence.

17. The storage controlling apparatus according to claim 13, wherein said interface buses are PCI (Peripheral Component Interconnect) buses.

18. The storage controlling apparatus according to claim 14, wherein said interface buses are PCI (Peripheral Component Interconnect) buses.

19. The storage controlling apparatus according to claim 15, wherein said interface buses are PCI (Peripheral Component Interconnect) buses.

20. The storage controlling apparatus according to claim 16, wherein said interface buses are PCI (Peripheral Component Interconnect) buses.

21. The storage controlling apparatus according to claim 17, wherein said interface buses are 64-bit PCI buses, said at least two different modes are a 64-bit transfer mode and a 32-bit transfer mode, said basic mode is said 64-bit transfer mode; and

when said determining means determines that said modes do not agree with each other, said notifying means determines that an inefficient transfer status occurs as said transfer mode abnormality, and notifies

of said error notice.

22. The storage controlling apparatus according to claim 18, wherein said interface buses are 64-bit PCI buses, said at least two different modes are a 64-bit transfer mode and a 32-bit transfer mode, said basic mode is said 64-bit transfer mode; and

when said determining means determines that said modes do not agree with each other, said notifying means determines that an inefficient transfer status occurs as said transfer mode abnormality, and notifies of said error notice.

23. The storage controlling apparatus according to claim 19, wherein said interface buses are 64-bit PCI buses, said at least two different modes are a 64-bit transfer mode and a 32-bit transfer mode, said basic mode is said 64-bit transfer mode; and

when said determining means determines that said modes do not agree with each other, said notifying means determines that an inefficient transfer status occurs as said transfer mode abnormality, and notifies of said error notice.

24. The storage controlling apparatus according to claim 20, wherein said interface buses are 64-bit PCI buses, said at least two different modes are a 64-bit

transfer mode and a 32-bit transfer mode, said basic mode is said 64-bit transfer mode; and

when said determining means determines that said modes do not agree with each other, said notifying means determines that an inefficient transfer status occurs as said transfer mode abnormality, and notifies of said error notice.

25. An interface module for a storage controlling apparatus disposed between a disk unit and a host to control an access from said host to said disk unit, said storage controlling apparatus comprising said interface module for controlling an interface with said disk unit or said host, a management module for generally managing the whole of said storage controlling apparatus, and a bridge module for connecting said interface module and said management module to each other so that data can be transferred between said interface module and said management module, said interface module comprising:

a first transfer processing unit for controlling data transfer between said interface module and said disk unit or said host;

a second transfer processing unit for controlling data transfer between said interface module and said bridge module;

said two transfer processing units being

connected to each other in at least two different modes through an interface bus so that data can be transferred between said two transfer processing units;

a determining means for determining whether or not a basic mode predetermined between said at least two different modes agrees with a mode set in a mode setting sequence executed when said interface module is reset or when data is transferred between said two transfer processing units; and

a notifying means for determining that transfer mode abnormality occurs when said determining means determines that said modes do not agree with each other, and for notifying of an error notice.

26. The interface module for a storage controlling apparatus according to claim 25 further comprising:

a controlling means for rerunning said mode setting sequence when receiving said error notice from said notifying means.

27. The interface module for a storage controlling apparatus according to claim 26, wherein when said determining means again determines that said modes do not agree with each other after said controlling means reruns said mode setting sequence, said notifying

means determines that a failure occurs, and notifies of a failure notice.

28. The interface module for a storage controlling apparatus according to claim 25, wherein when a confirmation signal responding to said basic mode remains disabled at the time of executing said mode setting sequence, said determining means determines that said modes do not agree with each other.

29. The interface module for a storage controlling apparatus according to claim 25, wherein said interface bus is a PCI (Peripheral Component Interconnect) bus.

30. The interface module for a storage controlling apparatus according to claim 26, wherein said interface bus is a PCI (Peripheral Component Interconnect) bus.

31. The interface module for a storage controlling apparatus according to claim 27, wherein said interface bus is a PCI (Peripheral Component Interconnect) bus.

32. The interface module for a storage controlling apparatus according to claim 28, wherein said

interface bus is a PCI (Peripheral Component Interconnect) bus.

33. The interface module for a storage controlling apparatus according to claim 29, wherein said interface bus is a 64-bit PCI bus, said at least two different modes are a 64-bit transfer mode and a 32-bit transfer mode, said basic mode is said 64-bit transfer mode; and

when said determining means determines that said modes do not agree with each other, said notifying means determines that an inefficient transfer status occurs as said transfer mode abnormality, and notifies of said error notice.

34. The interface module for a storage controlling apparatus according to claim 30, wherein said interface bus is a 64-bit PCI bus, said at least two different modes are a 64-bit transfer mode and a 32-bit transfer mode, said basic mode is said 64-bit transfer mode; and

when said determining means determines that said modes do not agree with each other, said notifying means determines that an inefficient transfer status occurs as said transfer mode abnormality, and notifies of said error notice.

35. The interface module for a storage controlling apparatus according to claim 31, wherein said interface bus is a 64-bit PCI bus, said at least two different modes are a 64-bit transfer mode and a 32-bit transfer mode, said basic mode is said 64-bit transfer mode; and

when said determining means determines that said modes do not agree with each other, said notifying means determines that an inefficient transfer status occurs as said transfer mode abnormality, and notifies of said error notice.

36. The interface module for a storage controlling apparatus according to claim 32, wherein said interface bus is a 64-bit PCI bus, said at least two different modes are a 64-bit transfer mode and a 32-bit transfer mode, said basic mode is said 64-bit transfer mode; and

when said determining means determines that said modes do not agree with each other, said notifying means determines that an inefficient transfer status occurs as said transfer mode abnormality, and notifies of said error notice.